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10/698,400	11/03/2003	Juhn Suk Yoo	8733.887.00-US	3427

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,400	YOO, JUHN SUK	
	Examiner	Art Unit	
	Grant D. Sitta	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: fig. 7 (34). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "126" [0099] four lines down from the top. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1 recites the limitation "the applied current" in claim 1, last line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-9, and 16-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et. al (2002/0005825) hereinafter, Lee.

8. In regards to claim 1, Lee teaches a data driver (fig. (24)) that outputs data signals formed using a substantially uniform current (fig. 4 signal from (Cd)); and a data signal controller circuit connected (fig. 12 (26, 28,30, 32)) to the data driver for charging a substantially uniform current (fig. 7) corresponding to the outputted data signals and for applying the outputted charged current corresponding to the outputted data signals (fig. 7), wherein light is emittable by the OELD panel in the presence of the applied current [0016].

9. In regards to claim 2, Lee teaches a scan driver (fig. 4 (22)) for applying scan signals to the OELD panel; and a timing controller for controlling the scan driver and the data driver (inherent).

10. In regards to claim 3, Lee teaches an OELD panel includes pixel cells (fig. 5) formed at crossings of gate lines (GL) and data lines (DL), wherein each pixel cell includes an electro luminescence cell (ELC) and a cell driver (26), wherein the cell

driver includes: a first switching device (MP1) formed between a cell drive voltage source and the electro luminescence cell (ELC) for driving the electro luminescence cell; a second switching device (MP2) connected to the cell drive voltage source (VDD) to form a current mirror (MP1, MP2 and C1) with the first switching device (MP1); a third switching device connected to the second switching device (MP3), a gate electrode line (GL), and a data line, wherein the third switching device (MP3) is responsive to data signals outputted by the data driver; a fourth switching device (MP4) connected to gate terminals of the second and third switching devices (MP4 is connected to each terminal), a data line, and the third switching device; and a storage capacitor (C1) connected between gate terminals of the first and second switching devices and the cell drive voltage source (N2).

11. In regards to claim 4, Lee teaches wherein the OELD panel includes pixel cells formed at crossings of gate lines and data lines (fig. 2 DL and GL), wherein each pixel cell includes an electro luminescence cell (ELC) and a cell driver (16), wherein the cell driver includes: a first switching device (MP1) formed between a cell drive voltage (VDD) source and the electro luminescence cell (ELC) for driving the electro luminescence cell; a second switching device (MP2) connected to the first switching device (MP1), a gate electrode line (GL), and a data line (DL), wherein the second switching device is responsive to data signals outputted by the data driver; and a storage capacitor (C1) connected between gate terminals of the first and second switching devices and the cell drive voltage source(VDD).

12. In regards to claim 5, Lee teaches a plurality of data lines (fig. 4 DL,DL,...DL) coupled between the data signal controller (24) circuit and the OELD panel (20).

13. In regards to claim 6, Lee teaches wherein the data signal controller circuit includes a plurality of constant current supply switching devices having gate terminals connected to a cell drive voltage source for applying the substantially uniform current to the data lines [0055].

14. In regards to claim 7, Lee teaches wherein the data signal controller circuit includes: a first data signal controller circuit (fig. 12 (28)) for storing a voltage corresponding to the data signals (fig. 12 (28)) outputted by the data driver during application of a first scan signal; a second data signal controller circuit (fig. 12 (30)) for storing a voltage corresponding to a data signal outputted from the first data signal controller circuit (fig. 12 (28)) and for applying the stored voltage to the data lines (DL) between application of the first scan signal (fig. 12) and a subsequent application of a second scan signal; a first switch connected between the data driver and the first data signal controller circuit for providing a current path between the data driver and the first data signal controller circuit (Examiner notes it is inherent to have a switch between the data driver that the "shift clock" controls); and a second switch connected between the first data signal controller circuit and the second data signal controller circuit for providing a current path between the first data signal controller circuit (Examiner notes a

second switch is also inherent otherwise the data would just be stored with no means to retrieve) and the second data signal controller circuit [0101].

15. In regards to claim 8, Lee teaches a data signal controller circuit (fig. 12) further includes a drive signal supplier (fig. 12 (32)) for driving the first (28) and second (30) data signal controller circuit.

16. In regards to claim 9, Lee teaches a shift register (fig. 12 (26)) for driving the first data signal controller circuit (28) and the first switch during (inherent) application of the first scan signal; and a line pass controller ([0101] data supplier) for driving the second data signal controller circuit (30) and the second switch (inherent) between application of the first scan signal and application of the second scan signal [0101].

17. In regards to claim 16, Lee teaches a driving method of an OELD panel (fig. 4) having pixel cells arranged at crossings of gate lines (GL) and data lines (DL), the method comprising: applying a first data signal from a data driver (24), wherein the first data signal is formed from a substantially uniform current [0054]; charging a first data signal controller circuit (fig. 12 signal to (28)) with a second data signal (fig. 2 (30)) corresponding to the substantially uniform current in response to the outputted first data signal [0055], wherein the first storage means (28) is controllable by a first drive signal during application (clock) of a first scan signal; charging a second data signal controller circuit (30) with a third data signal (Signal to CDB) corresponding to the substantially

uniform current in response to the second data signal, wherein the second data signal controller circuit (30) is controllable by a second drive signal ("shift clock") between the application of the first scan signal (26) and application of a second scan signal (signal from (28)); and applying the substantially uniform current [0101] to the data lines in response to the third data signal during application of the second scan signal [0102].

18. In regards to claim 17, Lee teaches wherein charging the first data signal controller circuit (fig. 12 (28)) with the second data signal includes (fig. 12 signal to (28)): forming a current path between the data driver (fig. 4 (24)) and the first data signal controller circuit (fig. 12 (28)) in response to the first drive signal (clock); inputting the first data signal from the data driver through the current path [0101]; and charging the first data signal controller circuit (fig. 12 (28)) with the second data signal corresponding to the substantially uniform current of the inputted first data signal [0101]-[0102].

19. In regards to claim 18, Lee teaches wherein charging the second data signal controller circuit (fig. 12 (30)) with the third data signal includes (fig. 12 signal from (28)): forming a current path between the first data signal controller circuit (fig. 12 (28)) and the second data signal controller circuit (fig. 12 (30)) in response to the second drive signal ("shift clock"); inputting the second data signal (fig. 12 signal from (28)) corresponding to a voltage charged in the first data signal controller circuit [0054]; and charging the second data signal controller circuit (fig. 12 (28)) with the third data signal

corresponding to the substantially uniform current of the inputted second data signal.[0101]-[0102]

20. In regards to claim 19, Lee teaches inputting the third data signal (fig. 12 (Signal to CDB) during application of the second scan signal (shift clock); charging a storage capacitor (fig. 5 (C1)) in the OELD panel in accordance with the inputted third data signal (fig. 12 (Signal to CDB) and controlling a current path width of a switching device (fig. 5 (MP1)) connected to an electro luminescence cell (fig. 5 (ELC)) within the OELD; and causing the electro luminescence cell to emit light in accordance with a voltage difference between a cell drive voltage source and a ground voltage source and in accordance with the current path width [0017] and (abstract).

21. In regards to claim 20, Lee teaches wherein a current characteristic of the first and second data signals are different from a current characteristic of the third data signal [0017].

22. In regards to claim 21, Lee teaches a data driver (fig. 4 (24)) for outputting data signals; a display panel comprising a substrate (fig. 4 (20)); and a data signal controller circuit, for controlling the output data signals ([0101], "controller"), the data signal controller circuit (fig. (12)) being formed on the substrate and coupled between the data driver and the display panel (fig. 4).

23. In regards to claim 22, Lee teaches wherein the data signal controller circuit further comprises a first data signal controller circuit (fig. 12 (28)), a second data signal controller circuit (fig. 12 (30)) coupled to the first data signal controller circuit and the display panel (Examiner notes the data signal controller must be coupled to the display panel).

24. In regards to claim 23, Lee teaches wherein the first data signal controller circuit fig. 12 (28) is selectively connectable to the second data signal controller circuit (fig. 12 (30)).

25. In regards to claim 24, Lee teaches wherein the data signal controller circuit (fig. 12 (26), (28), (30), (32)) is selectively connectable to the display panel (fig. 4 (20)).

26. In regards to claim 25, Lee teaches a plurality of organic electroluminescent pixel elements (fig. 4) within the display panel for expressing light, wherein luminosity values of the plurality of pixel elements across the display panel vary by less than about 30% (figs. 9, 10, and 11) Examiner notes Lee teaches a luminosity that does not vary and this is accomplished by supplying the current with a current mirror. Current mirrors keep a constant current regardless of loading.

27. In regards to claim 26, Lee teaches a data driver (fig. 4 (24)) for outputting data signals; and a data signal controller circuit (fig. 12 (26), (28), (30), and (32)), for

controlling the output data signals (fig. 4 signal to pixels), the data signal controller circuit being electrically coupled to the display panel and coupled between the data driver and the display panel (fig. 4 (CD)).

28. In regards to claim 27, Lee teaches wherein the data signal controller circuit (fig. 12 (26), (28), (30) and (32)) further comprises a first data signal controller circuit (28) and a second data signal controller circuit (30) coupled to the first data signal controller circuit and the display panel (fig. 4 (20)).

29. In regards to claim 28, wherein the first data signal controller circuit (fig. 12 (28)) is selectively connectable (Examiner notes switches in the latch will selectively determine whether the line is connected or disconnected) to the second data signal controller circuit (fig. 12 (30).

30. In regards to claim 29, Lee teaches wherein the data signal controller circuit is selectively connectable to the display panel (fig. 6 (MN11)).

31. In regards to claim 30, Lee teaches wherein the data signal controller circuit is formed on the display panel (fig. 4) [0052]-[0055].

32. In regards to claim 31, Lee teaches wherein the data signal controller circuit is mounted directly on the display panel (fig. 4) 0052]-[0055].

33. In regards to claim 33, see claim 26.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Koyama et al (7,151,511) hereinafter, Koyama.

36. In regards to claim 10, Lee discloses the limitations of claim 9

Lee differs from the claimed invention in that Lee does not explicitly disclose a fifth switching, a first capacitor and a third switching connected between the fifth and second switch.

However, Koyama teaches a system and method for first data signal controller circuit includes (fig. 4A (A1)): a fifth switching device (fig. 4B switch top left corner of (450)) connected between the cell drive voltage source (fig. 4B VDD) and the second switch (fig. 4 B (452)); a first capacitor connected (transistor come with parasitic capacitance) between a gate terminal of the fifth switching device and the cell drive

voltage source; and a third switch connected between the gate terminal of the fifth switching device and the second switch (fig. 4B upper right corner), wherein the third switch is controllable by the shift register (fig. 5 (SR). (col. 14, lines 18-70 of Koyama).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Lee to include the use of switching means and memory as taught by Koyama in order to reduce power consumption as stated in (col. 5, lines 32-45 of Koyama).

37. In regards to claim 11, Koyama teaches a second data signal controller circuit including: a sixth switching device (fig. 4b lower right corner) connected between the second switch (fig. 4 B upper left corner) and a ground voltage source (GND); a second capacitor connected between a gate terminal of the sixth switching device and the ground voltage source (transistor have parasitic capacitance); and a fourth switch (fig. 4b lower left corner) connected between the gate terminal of the sixth switching device (fig. 4b lower right corner) and the second switch (fig. 4 B upper left corner), wherein the fourth switch in controllable by the line pass controller (fig, 2 latch pulse).

38. In regards to claim 12, Koyama teaches wherein the first switch is controllable by the shift register (fig. 1 (108)).

39. In regards to claim 13, Koyama teaches wherein the second switch is controllable by the line pass controller (fig. 2 "latch pulse").

40. In regards to claim 14, Koyama teaches wherein at least one of the switching devices is provided as a p-type metal oxide semiconductor field effect transistor (MOSFET) (12A and B P-channel TFT).

41. In regards to claim 15, Koyama teaches wherein at least one of the switching devices is provided as an n-type metal oxide semiconductor field effect transistor (MOSFET) (Fig. 12 A and B N-channel TFT).

42. Claim 32 is rejected under 35 U.S.C. 103(a) as being obvious and unpatentable over Lee.

43. In regards to claim 32, Lee teaches wherein the data signal controller circuit is attached to a side portion of the display panel (fig. 4). Examiner notes it would have been an obvious matter of design choice to attach the data signal controller circuit to the side, since such a modification would have involved a mere change in the location of a component. A change in a location is generally recognized as being within the level of ordinary skill in the art.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

June 13, 2007

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER